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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,271	08/25/2000	Petro Estakhri	LEXA-00301	5878

28960 7590 11/30/2005

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EXAMINER	
TRAN, DENISE	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,271	ESTAKHRI ET AL.	
	Examiner	Art Unit	
	Denise Tran	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-13 and 27-49* is/are allowed.

6)☒ Claim(s) *14,19,20,25,26,50-54 and 60-66* is/are rejected.

7)☒ Claim(s) *15-18,21-24 and 55-59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *5/25/05*.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/3/05 has been entered.

2. The applicant's amendment filed 10/3/05 has been considered. Claims 1-66 are presented for examination.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 50, 54, and 55 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,772,274. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of US 6, 772, 274 teaches correlation blocks but does not explicitly teaches overhead blocks. It would have been obvious to one of ordinary skill in the art at the time the invention to consider the correlation blocks as overhead blocks because the correlation blocks store correlation data to control operation of memory.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 50, 60-63 and 65 are rejected under 35 U.S.C. 102(e) as being anticipated by Conley et al., U.S. Patent No. 6,426,893 (hereinafter Conley).

As per claim 50, Conley teaches a flash memory device (fig. 1, el.. 17, 11) for storing user data comprising a plurality of separate, independently addressable, independently programmable and independently erasable non-volatile physical memory blocks distinguishably defined by a plurality of physical block addresses (e.g., title, col. 2 line 55 to col. 3, line 10, fig. 12, overhead data blocks and user data blocks) including:

a plurality of dedicated data blocks for storing user data (e.g., fig. 12, user data blocks; col. 2 line 55 to col. 3); and

a plurality of consecutively addressed dedicated overhead blocks for storing overhead data including a first dedicated overhead block and a second dedicated overhead block (e.g., fig. 12, O.H. data blocks; col.15 line 63 to col. 16, line 65; col. 16, lines 1-17 or fig. 2, fig. 12, reserved, OH data blocks col. 16, lines 60-63; col. 17, lines 8-20); wherein the plurality of user data stored in dedicated data blocks being segregated from the plurality of overhead data stored in separate dedicated overhead blocks (e.g., fig. 12, 12, overhead data blocks and user data blocks; col. 2 line 55 to col. 3, line 10 or fig. 2, fig. 12, user data blocks and reserved, OH data blocks col. 16, lines 60-63; col. 17, lines 8-20).

As per claims 60-63 and 65, a controller for regulating and controlling the operation of the flash memory (e.g., fig. 1, el. 11, 39); a volatile RAM space manager, the space manager comprising a plurality of correlation fields for correlating virtual addresses and physical addresses (e.g., col. 17, line 25 to col. 18, line 35); the space manager comprises a flag register comprising a plurality of status flags (e.g., col. 16, lines 16-22; figs. 9-10); a means for loading data from a non volatile memory area into a correlation register of the RAM space manager on start up (e.g., col. 18, lines 1-10); and means for generating error correction data corresponding to user (e.g., fig. 1, el. 37).

7. Claims 14, 19-20, 25, 50-54, 60-63 and 65 are rejected under 35 U.S.C. 102(e) as being anticipated by Iida et al., U.S. Patent No. 6,625,713 B2 (hereinafter Iida).

As per claim 50, Iida teaches a flash memory device for storing user data comprising a plurality of separate, independently addressable, independently programmable and independently erasable non-volatile physical memory blocks distinguishably defined by a plurality of physical block addresses (i.e., segments or blocks, e.g., cols 5-6, figs. 7, 11 and 14) including:

a plurality of dedicated data blocks for storing user data (i.e., segments or blocks; e.g., figs. 7A and 11A segments or fig. 7A, blocks n-1 and n; col. 5, line 55 to col. 6, line 20; fig. 14B, main data blocks); and

a plurality of consecutive addressed dedicated overhead blocks for storing overhead data including a first dedicated overhead block and a second dedicated overhead block (i.e., segments or blocks; i.e., control data blocks storing overhead data, such as logical address 005, flag 0; figs. 7A and 11A segments or fig. 7A, blocks 0-3; fig. 7F; and col. 5, line 55 to col. 6, line 20; fig. 14C segments or block 123); wherein the plurality of user data stored in dedicated data blocks being segregated from the plurality of overhead data stored in separate dedicated overhead blocks (e.g., figs. 14A-D, control data blocks storing overhead data, such as logical address 005, flag 0 wherein the user data, main data, being segregated from the overhead data, logical address 005, flag 0 in separate blocks).

As per claim 14, Iida teaches a method of data storage within a flash memory comprising the steps:

Mapping a non volatile memory medium within the flash memory system into a plurality of independently addressable, independently programmable and independently erasable blocks (i.e., segments or blocks, e.g., cols 5-6, figs. 7, 11 and 14) including a plurality of dedicated data blocks (i.e., segments or blocks; e.g., figs. 7A and 11A segments or fig. 7A, blocks n-1 and n; fig. 14B, main data blocks; col. 5, line 55 to col. 6, line 20) and a plurality of dedicated overhead blocks comprising a first dedicated overhead block and a second dedicated overhead block (i.e., segments or blocks; i.e., control data blocks storing overhead data, such as logical address 005, flag 0; figs. 7A and 11A segments or fig. 7A, blocks 0-3; fig. 7F; and col. 5, line 55 to col. 6, line 20; fig. 14C segments or block 123);

Mapping each of the plurality of dedicated overhead blocks into a plurality of consecutive address overhead segments (e.g., figs. 14b-c, pages 0-15) wherein the plurality of segments within each dedicated overhead block are address according to an identical set of distinct segment addresses (e.g., figs. 14b-c, pages 0-15), each segment comprising: physical address register for storing a physical address for locating corresponding user data (e.g., fig. 14 D, 003; col. 12, lines 16-18); and a flag field (e.g., figs.14 B-C, control flag); and

Correlating the first Dedicated Overhead Block to a first group of virtual logical block addresses including a first VLBA (e.g., figs 14, redundant portion, logical address); wherein user data and overhead data are in separate blocks (e.g., figs. 14A-D, control data blocks storing overhead data, such as logical address 005, flag 0 wherein the user data, main data, being segregated from the overhead data, logical

address 005, flag 0 in separate blocks) such that the user data are stored in the plurality of dedicated data blocks and the overhead data are separately stored in the plurality of dedicated overhead blocks (e.g., figs. 14A-D, control data blocks storing overhead data, such as logical address 005, flag 0 wherein the user data, main data, being segregated from the overhead data, logical address 005, flag 0 in separate blocks).

As per claims 51-54, Iida teaches, wherein each dedicated overhead block is identically comprised of a plurality of separately addressable overhead pages, each block following an identical sequence of page addresses (i.e., blocks or pages; e.g., fig. 7A, blocks 1-3; or fig. 7D, pages 0-m); wherein each overhead page is comprised of a plurality of independently addressable and independently programmable segments (i.e., pages; e.g., fig. 7D, pages 0-m); wherein the plurality of independent overhead segments are used for storing overhead data, each overhead segment supporting one virtual logical block of user data (e.g., figs. 7E-F, redundant portion, logical address), each overhead segment comprising: physical address register for storing a physical address for locating corresponding user data (e.g., fig. 14 D, 003; col. 12, lines 16-18); and a flag field (e.g., figs.14 B-C, control flag); and Iida shows wherein a first group of virtual logical block addresses including a first VLBA are assigned to the first dedicated overhead block, such that overhead data generated in support of the first VLBA will be stored in an overhead segment within the first dedicated overhead block (e.g., figs 14, redundant portion, logical address).

As per claims 19-20, 25, 60-63 and 65, Iida shows a controller for regulating and controlling the operation of the flash memory (e.g., fig. 4, el. 109); a volatile ram space

manager comprising a plurality of correlation fields for correlating virtual addresses and physical addresses or storing a logical address within a non-volatile correlation register within the flash memory system (e.g., fig. 4, el. 111; and col. 13, lines 15-25 and col. 20, lines 30-35); the space manager comprises a flag register comprising a plurality of status flags (e.g., fig. 7F, status flags; fig. 14D, control table flags); a means for loading data from a non volatile memory area into a correlation register of the RAM space manager on start up or power up (e.g., col. 20, lines 30-35); means for generating error correction data corresponding to user (e.g., col. 7, lines 1-30

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al., U.S. Patent No. 6,625,713 B2 (hereinafter Iida) as applied to claim 50 above, and further in view of applicant's admitted prior art, the current specification pages 2-12 and figs. 1-6 (hereinafter AAPA).

As per claim 64, Iida shows a means for loading data from a nonvolatile memory area into the space manager on start up (e.g., col. 20, lines 30-35). Iida does not explicitly shows the use of a reset command. AAPA shows the use of a reset command (e.g., page 11, lines 20-26. It would have been obvious to one of ordinary skill in the art

at the time the invention was made to apply the teaching of AAPA into the system of Iida because it would allow the system to recover data from the system failure.

10. Claims 26 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al., U.S. Patent No. 6,625,713 B2 (hereinafter Iida) as applied to claims 50 or 14 above, and further in view of Tanaka, U.S. Patent No. 6,446177 B1 (hereinafter Tanaka).

As per claims 26 and 66, Iida shows a dedicated data block to function as a dedicated overhead block and an existing dedicated overhead block (e.g., col. 11, line 65- col. 12, line 15). Iida does not explicitly shows means for re-designating a block in the even of failure of an existing block. Tanaka shows means for re-designating a block in the even of failure of an existing block (e.g., page 28, lines 40-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Tanaka into the system of Iida because it would allow the system to recover data from the defective block.

11. Claims 1-13 and 27-49 are allowed.

12. Claims 15-18, 21-24, and 55-59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Applicant's arguments filed 10/3/05 have been fully considered but they are not persuasive.

14. In the remarks, the applicant argued that Conley failed to teach a flash memory device with a plurality of consecutively address dedicated overhead blocks.

The examiner disagreed with the applicant's arguments because Conley teaches a plurality of consecutively addressed dedicated overhead blocks for storing overhead data including a first dedicated overhead block and a second dedicated overhead block (e.g., fig. 12, O.H. data blocks; col.15 line 63 to col. 16, line 65; col. 16, lines 1-17 or fig. 2, fig. 12, reserved, OH data blocks col. 16, lines 60-63; col. 17, lines 8-20); wherein the plurality of user data stored in dedicated data blocks being segregated from the plurality of overhead data stored in separate dedicated overhead blocks (e.g., fig. 12, 12, overhead data blocks and user data blocks; col. 2 line 55 to col. 3, line 10 or fig. 2, fig. 12, user data blocks and reserved, OH data blocks col. 16, lines 60-63; col. 17, lines 8-20). In particular, col. 16, lines 1-7 teaches the block overhead records are logically arrange as a continuum of logical block addresses. Also, col. 16, line 5 to 20 teaches a reserved block is designated for OH data and contains control data.

15. In the remarks, the applicant argued that Iida failed to teach a flash memory with a plurality of consecutively addressed dedicated overhead data blocks segregated from the plurality of user data blocks in the flash memory array and segregating overhead data blocks from user data blocks in the flash memory array.

The examiner disagreed with the applicant's arguments because Iida teaches a plurality of consecutive addressed dedicated overhead blocks for storing overhead data including a first dedicated overhead block and a second dedicated overhead block (i.e., segments or blocks; i.e., control data blocks storing overhead data, such as logical address 005, flag 0; figs. 7A and 11A segments or fig. 7A, blocks 0-3; fig. 7F; and col. 5, line 55 to col. 6, line 20; fig. 14C segments or block 123); wherein the user data being segregated from the overhead data in separate blocks (e.g., figs. 14A-D, control data blocks storing overhead data, such as logical address 005, flag 0 wherein the user data, main data, being segregated from the overhead data, logical address 005, flag 0 in separate blocks). Also, Iida, figs. 7 shows overhead blocks 0-1 being segregating from data blocks n-1 and n.

16. In the remarks, the applicant argued that neither Iida, Tanaka, nor their combination teaches a flash memory with a plurality of consecutively addressed dedicated overhead data blocks which is segregated from the plurality of user data blocks from the plurality of overhead data blocks from user data blocks in separate memory blocks in the flash memory array.

The examiner disagreed with the applicant's arguments because Iida teaches a plurality of consecutive addressed dedicated overhead blocks for storing overhead data including a first dedicated overhead block and a second dedicated overhead block (i.e., segments or blocks; i.e., control data blocks storing overhead data, such as logical address 005, flag 0; figs. 7A and 11A segments or fig. 7A, blocks 0-3; fig. 7F; and col. 5,

line 55 to col. 6, line 20; fig. 14C segments or block 123); wherein the user data being segregated from the overhead data in separate blocks (e.g., figs. 14A-D, control data blocks storing overhead data, such as logical address 005, flag 0 wherein the user data, main data, being segregated from the overhead data, logical address 005, flag 0 in separate blocks). Also, Iida, figs. 7 shows overhead blocks 0-1 being segregating from data blocks n-1 and n. Therefore, the combination of Iida and Tanaka also teaches a flash memory with a plurality of consecutively addressed dedicated overhead data blocks which is segregated from the plurality of user data blocks from the plurality of overhead data blocks from user data blocks in separate memory blocks in the flash memory array.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday, Thursday, and an alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone numbers for

the organization where this application or proceeding is assigned are (571) 273-8300 for central Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9600.

D.T.
11/26/ 2005